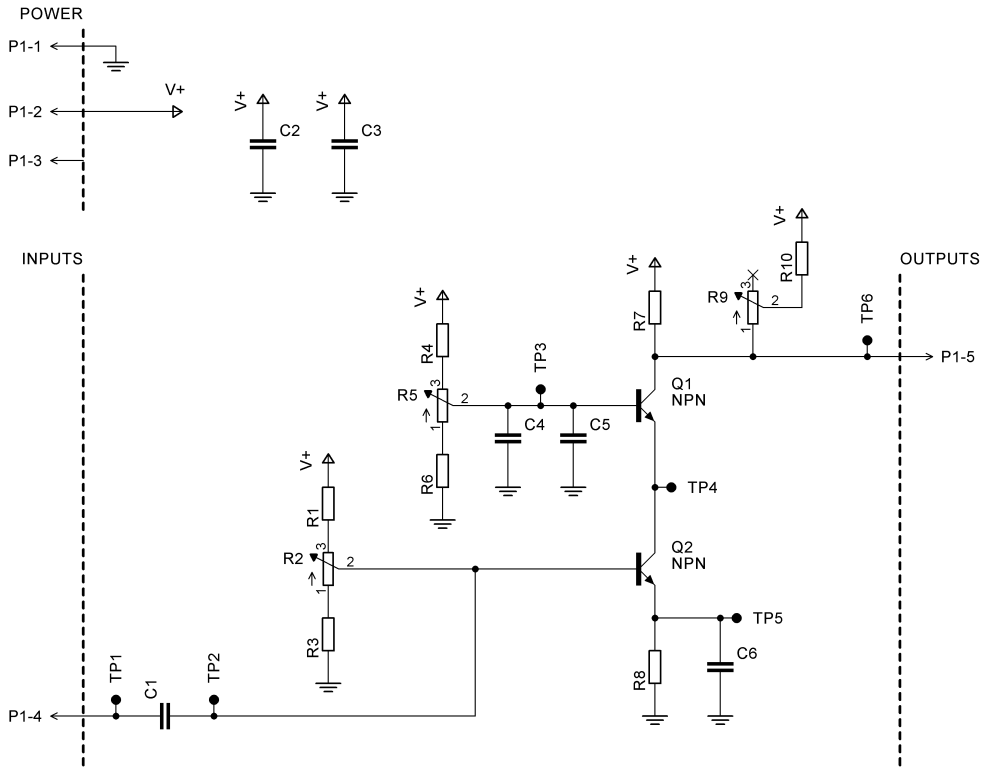
Cascode Amplifier

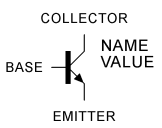
NOTES:



PART: NPN BIPOLAR JUNCTION TRANSISTOR

FOOTPRINT: TO92	EXAMPLE PART: 2N3904

SCHEMATIC SYMBOL



PINOUT

PIN	DESCRIPTION
1	EMITTER
2	BASE
3	COLLECTOR

TITLE: CASCODE AMPLIFIER

SIZE	DWG NO	REV
B	04B-340	A1-03

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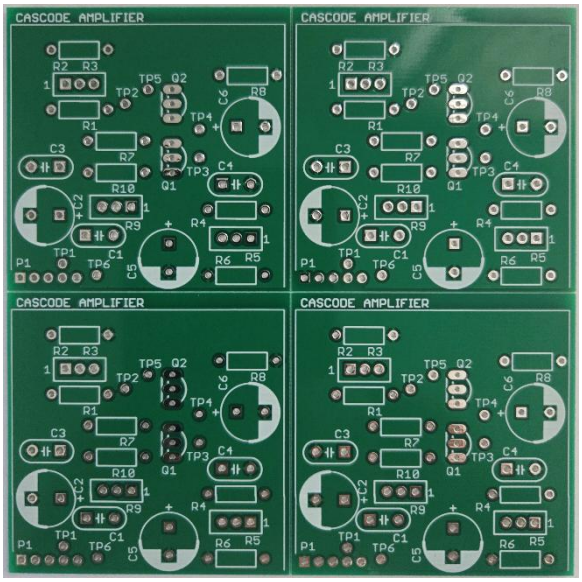
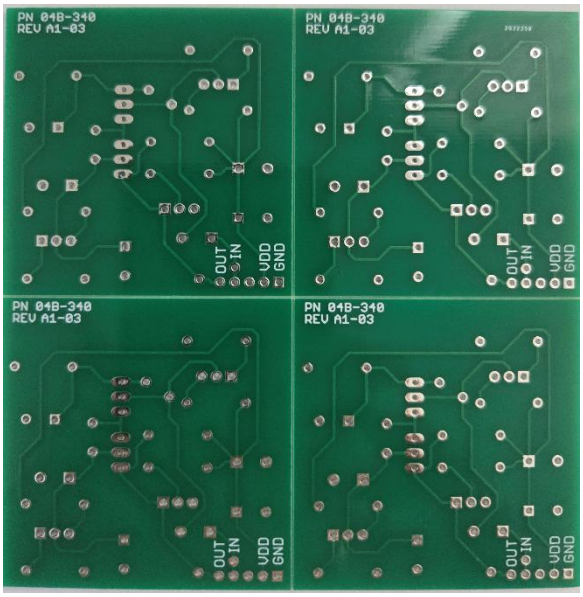


Front Side



Back Side

PART NO	TITLE	PIECES PER PANEL
04B-340	Cascode Amplifier	4

Ordering Information

Email me, nolan@minipcb.com, a list of the boards you'd like to buy, how many you want, when you want them delivered by, and a shipping address. We'll figure out what payment option and price works for you.

Circuit Description

This miniPCB implements a single-stage cascode amplifier using two discrete NPN bipolar junction transistors (Q1 and Q2) in a stacked configuration. The design can optionally accommodate N-channel MOSFETs in place of BJTs for comparative testing. The cascode topology combines a common emitter (Q2) and common base (Q1) stage to achieve high voltage gain, increased bandwidth, and improved isolation between input and output. This circuit is ideal for demonstrating the performance advantages of cascode operation, including reduced Miller effect and enhanced high-frequency response.

Input Coupling and Biasing – Q2 Stage

The AC input signal is coupled to the circuit through C1, a DC blocking capacitor that prevents source bias from interfering with the transistor's base. The input transistor Q2 is biased via a voltage divider consisting of R1, R2 (a multiturn trimmer), and R3, allowing precise adjustment of the base voltage and establishing the correct quiescent current. TP2 allows direct measurement of Q2's base voltage, while TP1 monitors the input signal level.

Power Supply Filtering

C2 and C3 are supply rail filtering capacitors that stabilize the positive voltage rail and suppress high-frequency noise. These components improve power integrity for both gain stages.

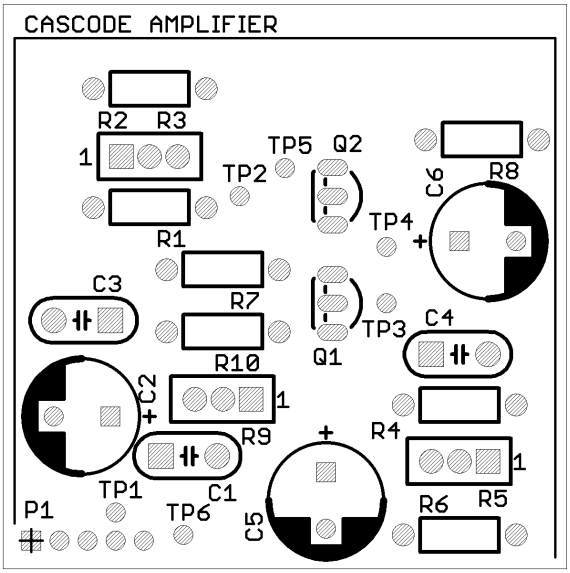


Figure 1 - Single Board, Component Outlines

Biasing of Q1 – Common Base Stage

The base of the output transistor Q1 is held at a fixed voltage determined by a voltage divider formed by R4, R5 (a multiturn trimmer), and R6. This sets the operating point for the common base stage. C4 and C5 are connected in parallel with the base bias node to stabilize the voltage and filter out noise or ripple, ensuring stable operation. TP3 allows direct probing of Q1's base voltage.

Collector and Interstage Connection

Q2's collector is directly connected to the emitter of Q1, forming the critical cascode connection between stages. TP4 is placed at this node to measure the intermediate collector-emitter junction between the two transistors. This connection minimizes voltage variation at Q2's collector, significantly reducing Miller capacitance and improving high-frequency gain.

Emitter Network – Q2 Stage

The emitter of Q2 is connected to ground through R8, providing a path for emitter current, while C6 is placed in parallel to allow AC signals to bypass the resistor and maintain high gain at signal frequencies. TP5 enables direct measurement of Q2's emitter voltage for DC bias or signal monitoring.

Output Stage – Q1 Collector

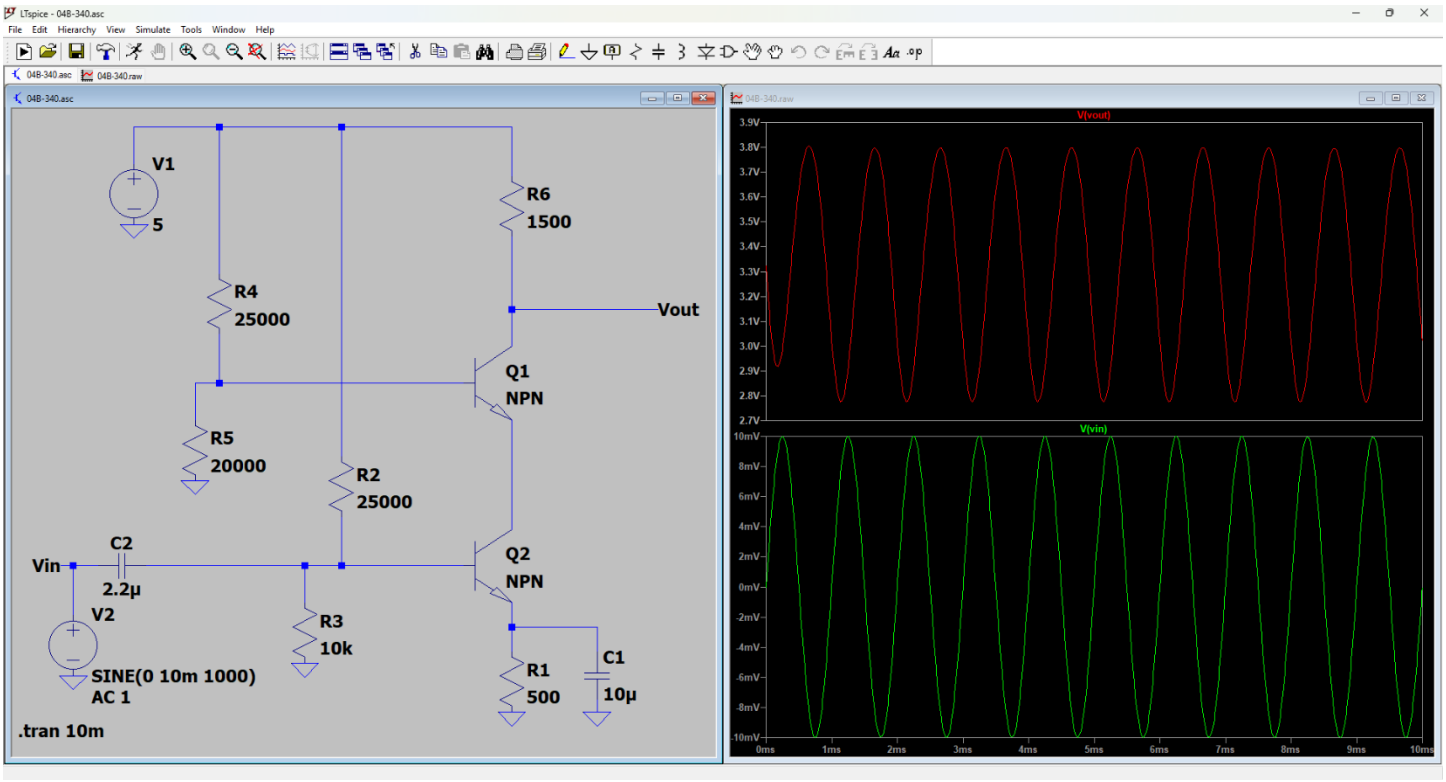
The collector of Q1 forms the output of the amplifier and is connected through a resistive load composed of R7, R9 (a multiturn trimmer), and R10. This network determines the output voltage swing and affects overall gain. Fine-tuning via R9 allows adjustment of the output bias point. TP6 allows measurement of Q1's collector voltage, which represents the final output signal of the amplifier.

Transistor Configuration

Both Q1 and Q2 are mounted in TO-92 footprints with a standard C-B-E (Collector–Base–Emitter) pinout. The layout is optimized for NPN BJTs, though many N-channel MOSFETs with matching pinouts are also compatible and can be used for substitution and experimentation. Most JFETs are not drop-in compatible due to differing pinouts and biasing requirements. This flexible design allows users to explore the advantages and tradeoffs of different transistor types within the cascode configuration.

Simulation in LTspice

LTspice was used to verify that selected component values produced reasonable amplifier behavior before assembling physical boards. The simulation helped confirm that the circuit was biased correctly, the signal was amplified, and the overall configuration functioned as expected with a voltage gain around 50. While the analysis wasn't exhaustive, the simulation served as a practical check to ensure the design was sound and worth building.



Parts List

REF DES	PART TYPE	VALUE / DESCRIPTION
C1	CAPACITOR	2.2uF
C2	CAPACITOR	10uF
C3	CAPACITOR	0.1uF
C4	CAPACITOR	0.1uF
C5	CAPACITOR	10uF
C6	CAPACITOR	10uF
R1	RESISTOR	15kΩ
R2	RESISTOR (TRIMMER)	25kΩ
R3	RESISTOR	10kΩ
R4	RESISTOR	10kΩ
R5	RESISTOR (TRIMMER)	25kΩ
R6	RESISTOR	15kΩ
R7	RESISTOR	3.3kΩ
R8	RESISTOR	500Ω
R9	RESISTOR (TRIMMER)	1kΩ
R10	RESISTOR	2.2kΩ
Q1	TRANSISTOR	2N3904
TP1-TP6	TEST POINT	KEYSTONE ELECTRONICS SERIES 5000
P1	HEADER PINS	5POS, 2.54mm PITCH, RA

Pictures of the Build

Testing Videos

Parts List (Form)

REF DES	PART TYPE	VALUE / DESCRIPTION
C1	CAPACITOR	
C2	CAPACITOR	
C3	CAPACITOR	
C4	CAPACITOR	
C5	CAPACITOR	
C6	CAPACITOR	
R1	RESISTOR	
R2	RESISTOR (TRIMMER)	
R3	RESISTOR	
R4	RESISTOR	
R5	RESISTOR (TRIMMER)	
R6	RESISTOR	
R7	RESISTOR	
R8	RESISTOR	
R9	RESISTOR (TRIMMER)	
R10	RESISTOR	
Q1	TRANSISTOR	
TP1-TP6	TEST POINT	KEYSTONE ELECTRONICS SERIES 5000
P1	HEADER PINS	5POS, 2.54mm PITCH, RA

Revision History

REV	DESCRIPTION	ECO	DATE
A	Initial Release		